AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (currently amended) An LSI semiconductor device comprising:

a plurality of processing elements; and

a single switcher that connects each of the plural processing elements to each other,

wherein each of the plural processing elements includes a network interface and is connected to the single switcher via the network interface,

wherein the plural processing elements are located at a plurality of sides of the single switcher,

wherein one of the plural processing elements and the single switcher are connected by peer-to-peer connection via at least one transmission line, [[and]]

wherein a connection path between said plural processors forms a system LSI, and

wherein the plural processing elements and the single switcher are implemented in a single semiconductor chip to form a chip LSI.

2. (canceled)

3. (previously presented) The semiconductor device of claim 1, wherein the switcher is located at the center position of the semiconductor device.

4. (canceled)

5. (previously presented) The semiconductor device of claim 1, wherein the plural processing elements and the single switcher are implemented in a single package.

6. (canceled)

7. (previously presented) The semiconductor device of claim 1, wherein each of the plural processing elements has a function of the same hierarchical level.

8. (currently amended) ~~The semiconductor device of claim 1,~~ An LSI semiconductor device comprising:

a plurality of processing elements; and

a single switcher that connects each of the plural processing elements to each other,

wherein each of the plural processing elements includes a network interface and is connected to the single switcher via the network interface,

wherein the plural processing elements are located at a plurality of sides of the single switcher,

wherein one of the plural processing elements and the single switcher are connected by peer-to-peer connection via at least one transmission line,

wherein a connection path between said plural processors forms a system LSI, and

wherein at least one of the plural processing elements and the single switcher are located in a space where light is confined, and each of the at least one of the plural processing elements and the single switcher has a light emitting element and a light receiving element, wherein an optical communication is performed between the at least one of the plural processing elements and the single switcher.

9. (currently amended) The semiconductor device of claim [[4]] 1 further comprising:

a plurality of semiconductor chips each of which includes plural processing elements and a single switcher; and

at least one inter-switcher which connects the semiconductor chips to each other.

10. (canceled)

11. (previously presented) The semiconductor device of claim 9, wherein the inter-switcher is located in one of the plural semiconductor chips, and the plural semiconductor chips are implemented on a plurality of stacked packages.

12. (previously presented) The semiconductor device of claim 9, wherein each switcher of the plural semiconductor chips and the inter-switcher is structured and arranged to have a circuit switching function.

13. (previously presented) The semiconductor device of claim 1, wherein each of the plural processing elements are only connected to the single switcher, through each respective network interface.

14. (canceled)

15. (canceled)

16. (previously presented) The semiconductor device of claim 8, wherein the light is confined by a sealing resin.

17-18. (canceled)